Electronic Version
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Claims

[c1] 1.A method for implementing backside probing of a semiconductor device, the method comprising:
isolating an identified defect area on a backside of the semiconductor device;
milling said identified defect area to an initial depth;
masking edges of said identified defect area;
etching unmasked semiconductor material within the semiconductor device, beginning at said initial depth, for a plurality of timed intervals until one or more active devices are reached; and
electrically probing said one or more active devices.

[c2] 2.The method of claim 1, further comprising backfilling a resulting cavity produced from said milling and said etching said backside of the semiconductor device.

[c3] 3.The method of claim 1, further comprising masking over-etched areas of said backside of the semiconductor device following one or more of said timed etching intervals.

[c4] 4.The method of claim 1, wherein said milling to an initial depth is implemented with a computerized milling

tool.

[c5] 5.The method of claim 4, wherein said initial depth results in a final thickness of about 60 to about 90 microns.

[c6] 6.The method of claim 1, wherein said etching further comprises a dry plasma etch utilizing sulfur hexafluoride (SF_6) at a flow rate of about 60 to about 100 standard cubic centimeters (SCCM) per minute, for a duration of about 2 to about 3 minutes.

[c7] 7.The method of claim 2, wherein said resulting cavity is backfilled with epoxy.

[c8] 8.The method of claim 3, wherein said masking said over-etched areas of said backside of the semiconductor device is implemented by covering exposed areas with carbon tape.

[c9] 9.A method for implementing backside probing of a semiconductor die, the method comprising:
isolating an identified defect area on a backside of the semiconductor die;
milling said identified defect area to an initial depth;
masking edges of said identified defect area;
etching unmasked semiconductor material, beginning at said initial depth, for a plurality of timed intervals until

one or more active devices are reached;
electrically probing said one or more active devices;
backfilling a resulting cavity produced from said milling and said etching said backside of the semiconductor device; and
cross sectioning the semiconductor device to locate one or more fail mechanisms associated therewith.

[c10] 10.The method of claim 9, further comprising masking over-etched areas of said backside of the semiconductor device following one or more of said timed etching intervals.

[c11] 11.The method of claim 9, wherein said milling to an initial depth is implemented with a computerized milling tool.

[c12] 12.The method of claim 11, wherein said initial depth results in a final thickness of about 60 to about 90 microns.

[c13] 13.The method of claim 9, wherein said etching further comprises a dry plasma etch utilizing sulfur hexafluoride (SF_6) at a flow rate of about 60 to about 100 standard cubic centimeters (SCCM) per minute, for a duration of about 2 to about 3 minutes.

[c14] 14.The method of claim 9, wherein said resulting cavity

is backfilled with epoxy.

[c15] 15.The method of claim 10, wherein said masking said over-etched areas of said backside of the semiconductor device is implemented by covering exposed areas with carbon tape.